

WHAT IS CLAIMED IS:

1 1. A process for determining the optimum load driving capacity for a driving  
2 node in a logic circuit comprising the steps of:

3 A) extracting the logic equations of the logic circuit from a circuit  
4 description thereof;

5 B) analyzing the fan-out of the driving node to determine if the total  
6 number of pass transistor loads is excessive compared to a  
7 predetermined driving capacity;

8 C) if, during step B), it is determined that the total number of pass  
9 transistor loads is exceeds an absolute maximum, then:

10 1) to the logic equations of the logic circuit, adding logic  
11 equations which represent the sum of the pass transistor loads;

12 2) to the logic equations of the logic circuit, adding comparator  
13 logic equations to compare the number of pass transistors turned  
14 on from one to the absolute maximum;

15 3) using a formal proof program to analyze the logic circuit and  
16 determine which of the comparators have a true output;

17 4) identifying the comparator for the largest number which has a  
18 possible true output to determine the highest possible actual  
19 load; and

20                   5) if necessary, adjusting the driving capacity of the driving  
21                   node to handle the determined highest possible actual load.

1    2. A process for determining the optimum load driving capacity for each  
2    driving node in a complex logic circuit comprising the steps of:

3           A) extracting the logic equations of the logic circuit from a circuit  
4           description thereof;

5           B) analyzing the fan-out of each driving node to determine if the total  
6           number of pass transistor loads of the analyzed node is excessive  
7           compared to a predetermined driving capacity;

8           C) for each driving node flagged during step B:

9                1) to the logic equations of the logic circuit, adding logic  
10                equations which represent the sum of the driving node's pass  
11                transistor loads; and

12               2) to the logic equations of the logic circuit, adding comparator  
13                logic equations to compare the number of pass transistors turned  
14                on from one to the absolute maximum for the driving node;

15           D) using a formal proof program to analyze the logic circuit and  
16           determine which of the comparators have a true output;

17           E) for each flagged driving node:

18                   1) identifying the comparator for the largest number which has a  
19                   possible true output to determine the highest possible actual load  
20                   for the driving node; and  
21                   2) if necessary, adjusting the driving capacity of the driving  
22                   node to handle the determined highest possible actual load.

1    3. A process for determining the required load driving capacity for a driving  
2    node in a logic circuit comprising the steps:

3           A) obtain a logical description of an electronic circuit;

4           B) identify logic nodes for further analysis within the circuit which are  
5           driven by gates that have variable loading dependent on the logical  
6           state of the logic circuit during operation;

7           C) develop added logical equations which describe arithmetically the  
8           loading on the driving gate as it depends on the logical value of other  
9           nodes in the logic circuit; and

10          D) use a program which implements formal mathematical methods of  
11          logical proof to determine the largest driving capacity required of the  
12          driving node by examining the outputs of the equations added to the  
13          logic to determine the largest actual loading that can be logically

14 placed upon the driving gate with consideration as to the possible  
15 overall logical state of the logic circuit.

1 4. The process of Claim 3 wherein the logical description of the electronic  
2 circuit is developed by a program that extracts the logical description from an  
3 electronic description of the circuit describing the interconnection of  
4 transistors and other electronic elements.

1 5. The process of Claim 4 including the added step in which the electronic  
2 circuit is modified to adjust the driving capacity of at least one node based  
3 upon the results of the formal proof process.

1 6. The process of Claim 3 wherein the added logic equations utilize integer  
2 values for specifying and calculating the loading.

1 7. The process of Claim 4 wherein the added logic equations utilize integer  
2 values for specifying and calculating the loading.

1 8. The process of Claim 5 wherein the added logic equations utilize integer  
2 values for specifying and calculating the loading.

1 9. The process of Claim 3 in which that analysis of logic nodes is further  
2 restricted to only those nodes identified in preliminary analysis as being in

- 3 violation of requirements based upon absolute worst case loading without
- 4 consideration as to the logical state of the logic circuit.